UDK3 Board Manager

The Cesys UDK3 Board Manager is a tool to handle various management tasks with UDK3 compatible devices like FPGA design download and flash programming.

Introduction

UDK3 Board Manager is a tool to perform generic tasks with UDK3 based devices. It can be used to:

- Display device data.
- Download FPGA design to device.
- Reset FPGA.
- Erase Flash memory.
- Program Flash memory.
- Define User ID.
- Convert FPGA designs to source files.

FPGA design format

The file format for FPGA-Designs is .bin (not .bit !). With ISE, check option **Create binary configuration file** in **Programming File / Process Properties**.

To convert a .bit to .bin using the SDK, choose **Xilinx Tools / Launch Shell**. Change to the directory of the .bit and call **promgen -u 0 [design].bit -p bin -spi -w** , where **[design].bit** is the input file, and **[design].bin** is generated.

Main Screen

The main screen shows information about the currently opened device and offers access to most functions through its toolbar.
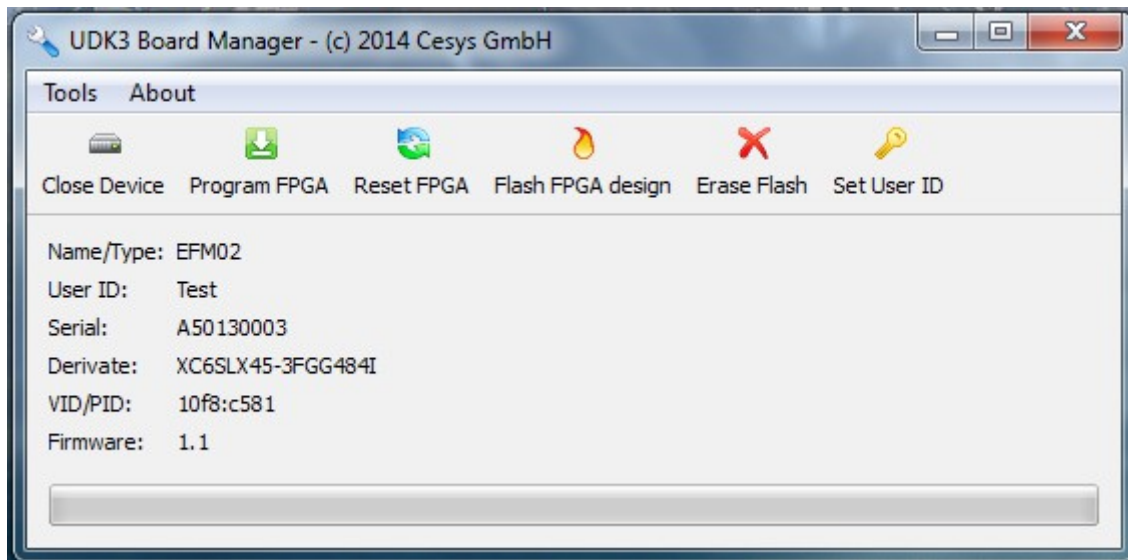
To work with a Cesys FPGA board or module, use the mixed **Open Device** / **Close Device** button. If it shows the text **Close Device**, a device is currently opened. UDK3 Board Manager does **not** detect if the device is unplugged if it is opened.

Use **Program FPGA** to open a file dialog an to select a design file. The FPGA will be configured using the selected design.

Reset FPGA activates the dedicated reset I/O of the FPGA for some milliseconds.

Flash FPGA design shows a file selection dialog for FPGA bistreams. The flash memory must be erased before a new design can be programmed. The application will asks if erase should be done before downloading the design. A message box indicates the completion. Don't close the application or unplug the device during this process. Depending on the flash size, this process can take some minutes.

Erase Flash resets the flash to factory defaults. Don't close the application or unplug the device during this process. Depending on the flash size, this process can take some

minutes.

Set User ID let's input a short text that is written to the device EEPROM (not flash). This ID is useful to differentiate devices of the same type. This ID is accessible from the API as well.

Convert FPGA bitstreams to source code

This dialog is accessible from Tools menu, It generates source code from FPGA bitstreams. This is useful to embed bitstreams into your sources to compile them into a executable.
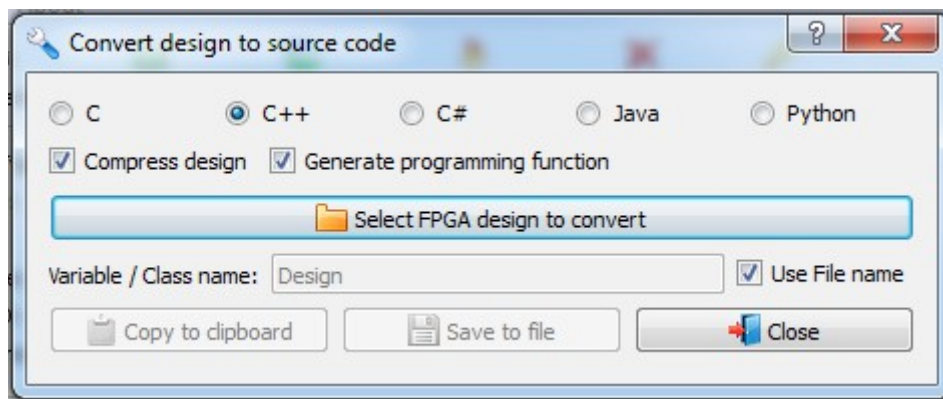
The code is created in the syntax of the language that is selected.

Compress design should always be enabled, this compresses the design using libz.

Generate programming function create a function or method that downloads the design. If this is not selected, only the design data is put into the source. Select FPGA design to convert opens a file dialog to choose the .bin file for conversion.

The name in the **Variable / Class name** field is used for variables in the source code. If **Use File name** is selected, the file name of the FPGA file is used instead. The name for the variable is not verified, choose a valid name.

After a design file is chosen, **Copy to clipboard** and **Save to file** are enabled.

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Revision history

v1.0	February, 17 2014	Initial release.
V1.1	May, 13 2014	Fpga .bin generation described.

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