

# **BeastLink Performance Monitor**

The BeastLink Performance Monitor is a tool to measure data transfer speeds between a host PC and BeastLink compatible devices. It can also test data integrity by performing write-readback-compare loops.

☑ Free Edition

☑ Pro Edition



### Introduction

BeastLink Performance Monitor is a tool that helps to maximize the data transfer rate with BeastLink-compatible devices. It can be used to locate bottlenecks and errors in the devices FPGA designs.

The tool configures the FPGA of the device using a user defined bitstream and transfers data to and from a specified address range. It displays the maximum data throughput while continuous transferring the data. There is a selectable option to verify data when using bi-directional communication. It is a good idea to select an address range that maps to BRAM, DDR2 SDRAM or other memory resource of the FPGA board when selecting "Verify".



## Options

The image below shows the BeastLink Performance Monitor.

BeastLink Performance Monitor - (c)	2018 Cesys GmbH	. o x		
VID/PID:	10f8 c583	Input		
FPGA design file:	./beastlink_exdes_top.bin	Output		
Area base address:	0x0000000	verity		
	Const address			
Area size:	0×100000	Random		
Transfer block size:	0×100000	Zero		
	2 KB 8 KB 64 KB 256 KB 1 MB	One Zero / One		
	Min: 306,31, Max: 307,81, Delta: 1,50 MB/s	• x 1		
300,00 MB/s		💿 x 4		
		© x 16		
		© x 64		
200,00 MB/s		_		
100.00 MB/s				
100,00 (10)5				
🕖 Stop	Serial: B20171894   UserId:			
🔍 About	Derivate: XC7A200T-2FBG676I   V:P: 10f8:c583   Firmware: 1.3.0			
🚺 About Qt	207 500 MP/c (min: 206 000 MP/c may: 200 000 MP/c)			
	2,064 GB, 00:00:06			

The **VID/PID** allows the selection of the device to run the test with. Default values are VID/PID from EFM-03 devices. The test will use the first device found during enumeration.

**FPGA design file** must contain the path to the bitstream file. The button right of the input control opens a file browser to ease the selection.

Area base address and Area size specify the area to which data is written and / or read from. Every single transfer is done using a block size as specified in **Transfer block size**. Data is transferred starting to / from the **Area base address** and continued at **Area base address + Transfer block size** and so on until **Area size** is reached. This is the reason why **Area size** 



must be a multiple of **Transfer block size**.

Values in these fields are interpreted as decimal, except they are prefixed using 0x, in which case the values are expected to be hexadecimal.

If **Const address** is checked, data is always transferred to / from Area base address only and the const address flag is used. Use the buttons directly below **Transfer block size** to set these values to common sizes.

**Input and Output** check boxes define the direction of the transfer. Direction is interpreted from host side. Either one or both options must be selected. If both are selected, **Verify** is a valid option.

**Random, Zero, One** and **Zero / One** define the content used for transfer. **Random** is randomly generated data, **Zero** are just buffers filled with 0. **One** and **Zero / One** must be interpreted as bits in this context. **One** means buffers filled with 0xFFFFFFF. **Zero / One** uses alternating bit patterns per 32 bit data line (0xFFFFFFF / 0x0000000) to produce a maximum toggle rate on the data lines.

The factors right of the performance graph (**x 1, x 4, x 16, x 64**) are pure visualization related options and specify the time factor of the graph.

The **Start / Stop** button switches between idle and running state. Starting a new test uses the currently selected options. Changing the options while a test is running, will not affect the test.



## **Revision history**

Version	Date	Comment	Author	Approved
1.0	Feb, 26 2018	Initial release	th	mr



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